# A High Efficiency Feedforward Amplifier with a Series Diode Linearizer for Cellular Base Stations

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***Abstract* — A feedforward power amplifier (FFPA) with a series diode linearizer using a bias feed resistance is presented. To improve overall feedforward amplifier efficiency, a series diode linearizer is used to provide main amplifier linearization. FFPA efficiency optimization design considering FET efficiency and linearity trade-off have been demonstrated. The developed FFPA achieved the high efficiency of 10% and output power of 45.6dBm at 10MHz offset ACLR –50dBc under W-CDMA 2 carriers signal.**

## I. INTRODUCTION

A feedforward power amplifier (FFPA) [1]-[6] has been widely used in cellular base stations, because of its high linearity and broad bandwidth performance. However, it has a disadvantage of low efficiency due to the need of an additional power amplifier in a distortion cancellation loop. So, the efficiency of FFPA is becoming significant concern in the design because of the limitation of current capacity in the base station system. To improve overall FFPA efficiency, the optimization of coupling coefficients of couplers have been reported [3]-[4]. In the FFPA, the most of DC input power is consumed by the main and error amplifiers. Therefore, the reduction of each amplifier's consumption power is important as well as the optimization of the passive circuit parameters. To decrease the overall FFPA consumption power, the improvement of main amplifier efficiency and linearity are required, respectively. The main amplifier linearity improvement decreases the consumption power of the error amplifier. However, it is difficult to improve both efficiency and linearity of the amplifier simultaneously, because of its trade-off.

Hybrid linearization is one solution to improve the overall FFPA performance. For example, two stage feedforward [1], feedforward with RF feedback [5], and feedforward with pre-distortion [6] have been reported. Considering the efficiency and bandwidth problems, a low loss and stable configuration, such as pre-distortion, is preferable. A parallel diode linearizer has been reported for a miniaturized FET linearizer [7]. This linearizer is effective for Class-A and Class-AB FET amplifiers.

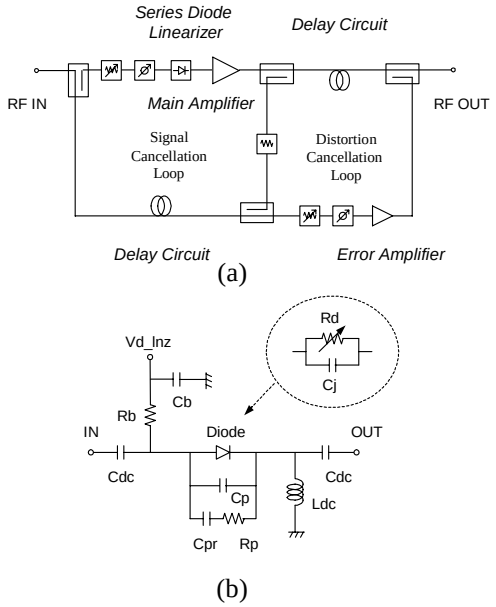


Fig. 1. Schematic diagram of a feedforward amplifier with a series diode linearizer. (a) A feedforward amplifier with a series diode linearizer. (b) A series diode linearizer.

This paper proposes a FFPA with a series diode linearizer using a bias feed resistance. This FFPA utilizes a series diode linearizer for enhancement of overall FFPA efficiency. The series diode linearizer has negative gain and positive phase deviations, so it is effective for linearization of Class-B high efficiency operated FET amplifier. Furthermore, FFPA efficiency optimization design considering FET efficiency and linearity trade-off are demonstrated. Finally, the overall performances of the developed FFPA with and without the series diode linearizer are compared.

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## II. CONFIGURATION

Fig. 1(a) shows the schematic diagram of a FFPA with a series diode linearizer. Both pre-distortion and adaptive feedforward linearization techniques are used in this FFPA. A series diode linearizer is utilized for the main amplifier linearization. The source and load impedance of FET have been determined considering overall FFPA efficiency. Fig. 1(b) shows the schematic diagram of a series diode linearizer. It consists of a series Schottky diode, a bias feed resistance *Rb*, a RF block inductance *Ldc* and DC block capacitors *Cb*, *Cdc*, *Cpr*. A parallel RC circuit *Cp*, *Rp* is used for adjusting the nonlinear characteristics of the linearizer.

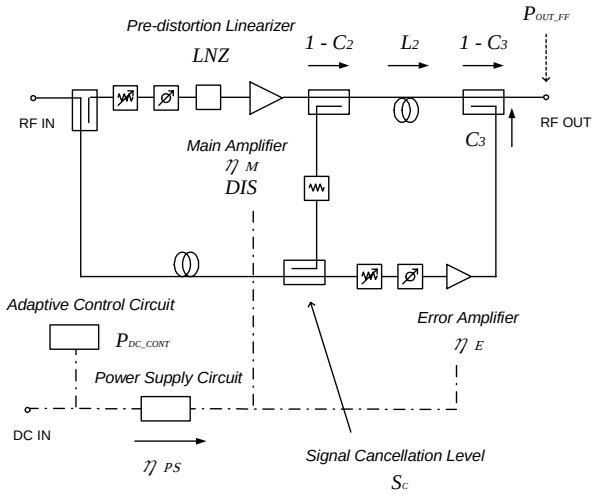



Fig. 2. Efficiency analysis model of a feedforward amplifier with a pre-distortion linearizer.

## III. EFFICIENCY OPTIMIZATION DESIGN

### *A. Main Amplifier*

The analysis of the overall FFPA efficiency and efficiency optimization design of a main amplifier are demonstrated. Fig.2 shows an efficiency analysis model of a FFPA with a pre-distortion linearizer. The FFPA efficiency $\eta_{FF}$ can be expressed as

$$\eta_{FF} = \frac{P_{OUT\_FF}}{P_{DC\_M} + P_{DC\_E} + P_{DC\_CONT}} \tag{1}$$

where

$$P_{DC\_M} = \frac{P_{OUT\_FF}}{(1-C_2)\cdot L_2 \cdot (1-C_3)\cdot \eta_{PS} \cdot \eta_M} \tag{2}$$

$$P_{DC\_E} = \frac{P_{OUT\_FF} \cdot (DIS \cdot LNZ + S_C)}{C_3 \cdot \eta_{PS} \cdot \eta_E} \tag{3}$$

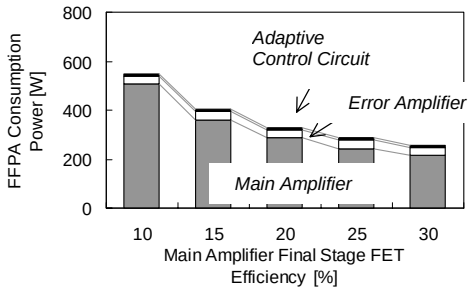
| | |
|---|---|
| $P_{OUT\_FF}$ | : output power of the FFPA |
| $P_{DC\_CONT}$ | : consumption power of the adaptive control circuit |
| $C_2$, $C_3$ | : coupling coefficients of the couplers |
| $L_2$ | : loss of delay circuit |
| $\eta_{PS}$ | : efficiency of the power supply circuit |
| $\eta_M$ | : efficiency of the main amplifier |
| *DIS* | : ratio of distortion power to output power of the main amplifier |
| *LNZ* | : distortion compensation level of the pre-distortion linearizer |
| $S_C$ | : signal cancellation level of the loop |
| $\eta_E$ | : efficiency of the error amplifier |

In this analysis, we use the following two assumptions. The first assumption is that amplifiers keep the constant back-off level. For example, 10 dB back-off for the main amplifier and 20 dB back-off for the error amplifier. These back-off levels must be determined carefully considering overall FFPA linearity. The second assumption is that the distortion power generated by the error amplifier and the residual power due to the imperfect cancellation of the distortion cancellation loop is negligibly small compared to the total output power of FFPA. Using Eqs.(1)-(3), we can determine the optimum FFPA parameters to maximize the FFPA efficiency.

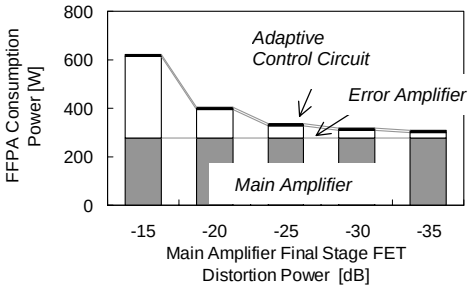
Fig.3 shows the calculated FFPA consumption power as a function of efficiency and linearity of the main amplifier FET. The efficiency improvement of the main amplifier FET directly decreases the main amplifier consumption power [see Fig.3(a)]. On the other hand, the linearity improvement of the main amplifier FET decreases the error amplifier consumption power [see Fig.3(b)]. However, in the practical design, it is difficult to improve both efficiency and linearity of the amplifier simultaneously, because of its trade-off. For example, a Class-B FET amplifier shows high efficiency and nonlinear characteristics. On the other hand, a Class-A FET amplifier shows low efficiency and linear characteristics.

Fig. 4 shows the calculated FFPA efficiency versus bias current of the main amplifier final stage FET. The bias current of the FET is normalized by the saturated drain current of the gate-source voltage *Vgs = 0V* (Idss). In this calculation, measurement results of a single stage 150W GaAsFET push-pull amplifier have been used. A single carrier W-CDMA modulated signal has been used as input signal. There is the optimum bias point to maximize the FFPA efficiency. The FFPA efficiency increases with

increasing the distortion cancellation level of the pre-distortion, particularly at low current operation. In the design, we have considered the distortion cancellation level of the series diode linearizer, and determined the optimum bias point to maximize the FFPA efficiency.




(a)




(b)

Fig. 3. Calculated FFPA consumption power versus main amplifier final stage FET characteristics. (a) FFPA consumption power versus efficiency of a FET. (b) FFPA consumption power versus distortion power of a FET.

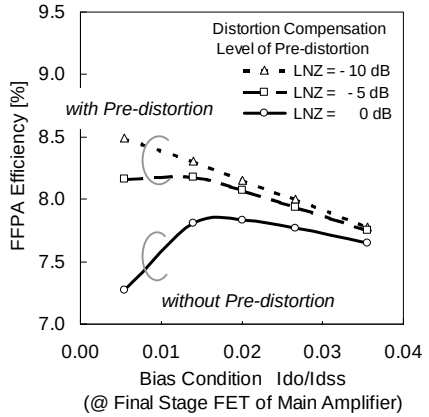



Fig. 4. Calculated FFPA efficiency versus bias current of a main amplifier final stage FET at W-CDMA 1 carrier signal.

*B. Series Diode Linearizer*

Nonlinear characteristics of a series diode linearizer are presented. If we express a diode as an equivalent circuit of an equivalent resistance *Rd* and a junction capacitance *Cj* [see Fig.1(b)] gain and phase of the series diode linearizer are approximately given as

$$|S21| = \frac{2Z_0\left(1+\omega^2C^2R^2\right)}{\sqrt{\left\{2Z_0\left(1+\omega^2C^2R^2\right)+R\right\}^2+\omega^2C^2R^4}} \tag{4}$$

$$\angle S21 = \tan^{-1}\left\{\frac{\omega CR^2}{2Z_0\left(1+\omega^2C^2R^2\right)+R}\right\} \tag{5}$$

with

$$1 >> \frac{Z_0}{R_b}, \quad C = C_j + C_p, \quad R = \frac{R_d R_p}{R_d + R_p} \tag{6}$$

where *Zo* is the characteristics impedance. Fig.5 shows the calculated gain and phase of the series diode linearizer. In this linearizer, *Rd* increases with increase of RF input power. Therefore, this linearizer achieves negative gain and positive phase deviations with increase of RF input power. In general, a Class-B FET amplifier has the positive gain and negative phase deviations with the increase of RF input power. Therefore, this linearizer is suitable for linearization of a Class-B FET amplifier.

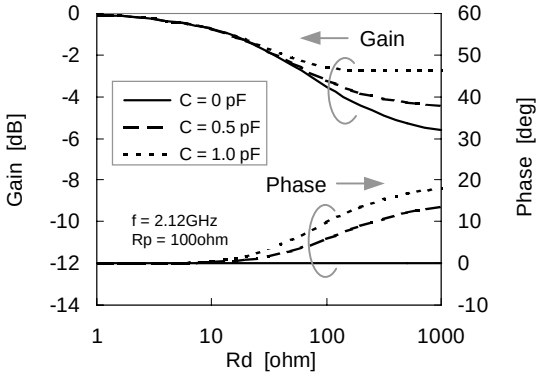



Fig. 5. Calculated gain and phase characteristics of the series diode linearizer.

## IV. Experimental Results

The overall performances of the FFPA have been measured. Fig. 6 shows the measured 10MHz offset adjacent channel leakage power ratio (ACLR) and overall FFPA efficiency at W-CDMA 2 carriers signal. The center and offset frequency of the input signal are 2.12GHz and 10MHz. Fig. 6(a) presents the ACLR and efficiency of the conventional FFPA. The efficiency and output power of 9% and 45.2dBm have been obtained at 10MHz offset ACLR –50dBc. Fig. 6(b) shows the ACLR and efficiency of the developed FFPA with the series diode linearizer. The efficiency and output power of 10% and 45.6dBm have been achieved at 10MHz offset ACLR –50dBc. The efficiency enhancement of 1% has been obtained by using the series diode linearizer in the FFPA.

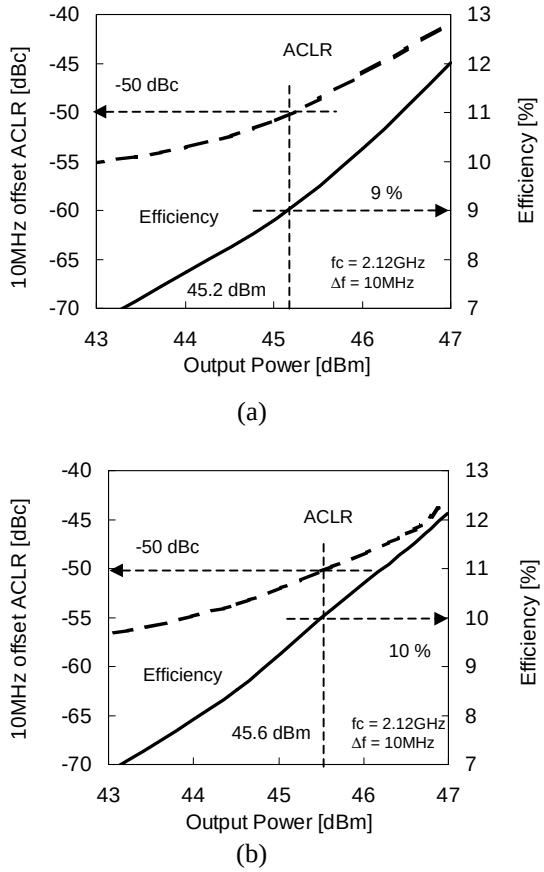



Fig. 6. Measured 10MHz offset ACLR and efficiency of the feedforward amplifier at W-CDMA 2 carriers signal. (a) The conventional feedforward amplifier. (b) The feedforward amplifier with the series diode linearizer.

## V. Conclusions

A FFPA with a series diode linearizer using a bias feed resistance is presented. To improve overall FFPA efficiency, a series diode linearizer has been used to provide main amplifier linearization. FFPA efficiency optimization design considering FET efficiency and gain trade-off have been demonstrated. From measured overall performances of the FFPA, the efficiency enhancement of the series diode linearizer has been shown. The developed FFPA achieved the high efficiency and output power of 10% and 45.6dBm at 10MHz offset ACLR –50dBc under W-CDMA 2 carriers signal.

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